REMARKS

Applicant has carefully reviewed and considered the Final Office Action mailed on July 31, 2007, and the references cited therewith.

Claims 1, 16, 26, 38, 47, and 55 are amended, no claims are canceled, and no claims are added; as a result, claims 1-6, 8-33, and 36-59 are now pending in this application.

§ 112 Rejection of the Claims

Claims 47-49 and 55-57 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Applicant respectfully traverses the rejections as follows.

The Office Action appears to consider "alignment" in the absolute, wherein two structures either are, or are not, arranged in complete alignment, and thus finds the term "partially aligned" unclear. Applicant submits that "partial alignment" refers to some portion of a first element/structure being aligned with, e.g., overlapping as taken in a vertical direction, some portion of a second element/structure. In other words, Applicant's claims encompass some offset from perfect alignment of the claimed elements/structures.

In claiming certain elements/structures are "at least partially aligned" with other claimed elements/structures, the entire first element/structure need not necessarily be completely aligned with the entire second element/structure. It is sufficient to have some portion of each of the respective elements/structures to be arranged in alignment to obtain the desired operability. Applicant's claimed invention is not to be limited to elements/structures being in perfect, complete, or entire alignment. One skilled in the art of multi-layer memory integrated circuit fabrication will appreciate that patterned elements/structures need not be perfectly aligned to be operable, and indeed, perfect alignment of integrated circuit structures is not absolute, and difficult to achieve in

practice. Rather it is sufficient to have fabricated structures be in partial alignment, for example substantial alignment, with one another so as to make them operable.

The desired operability of the features of the present disclosure being formed is understood by those having ordinary skill in the art. Considering the practicalities of precisely fabricating integrated circuit structures, one having ordinary skill in the art will understand the term "partially aligned" as applied to forming a second conductive layer being at least partially aligned with the middle electrode, and memory cells of each set being at least partially aligned vertically with each other. Alignment of these features is adequately illustrated in the drawings, and some offset from perfect alignment, e.g., partial alignment. Thus the term "partial aligned" is not unclear to one skilled in the art. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the 112 rejection of claims 47-49 and 55-57.

§ 103 Rejection of the Claims

Claims 1, 3-6, 8-11, 16, 26-33, 38-41, 47-49 and 55-59 were rejected under 35 USC § 103(a) as being unpatentable over Miyasaka (U.S. Patent No. 4,476,547) in view of Udayakumar et al. (U.S. Publication No. 2005/0012126).

Applicant respectfully traverses the rejections as follows.

With regard to independent claims 1, 16, 26, 38, 47, and 55, the Applicant submits that the Miyasaka and Udayakumar references, alone or in combination, do not describe, teach, or suggest each and every element provided in Applicant's independent claims. Page 3 of the Office Action mailed July 31, 2007 acknowledges "Miyasaka does not teach that each control element including a silicon-rich oxide insulator," and suggests the Udayakumar reference teaches "a memory cell Cfe having . . . a control element wherein the control element including a silicon-rich oxide insulator SILOX2." The Office Action further suggests "It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a silicon-rich oxide insulator in

each control element of Miyasaka's device in order to improve the characteristic's of the device" (emphasis added).

Applicant respectfully disagrees with this characterization of the Udayakumar reference, and submits that it does not teach a memory cell having a control element wherein the control element including a silicon-rich oxide insulator. Paragraphs 0032 – 0034 of the Udayakumar reference, along with Figure 4A, appear to describe fabrication of a control element embodiment, e.g., a transistor. However, nowhere does the Udayakumar reference describe, teach, or suggest the control element, e.g., transistor, includes a silicon-rich oxide insulator.

While the Udayakumar reference appears to teach a particular use of a silicon-rich oxide insulator, the particular use of the silicon-rich insulator is for a very specific purpose unrelated to the control element, e.g., formed over a hydrogen barrier above a specific type of capacitor to prevent or mitigate degradation of the capacitor ferroelectric materials due to exposure to hydrogen in back-end processing in many CMOS integration schemes (see paragraphs 0021 and 0023 of the Udayakumar reference). Paragraph 0035, along with Figures 4B – 4G, of the Udayakumar reference appears to describe fabrication of one embodiment of ferroelectric capacitors. Fabrication of another embodiment of ferroelectric capacitors appears to be described in conjunction with Figures 7A – 7F of the Udayakumar reference. A first hydrogen barrier, e.g., AlOx, and a second hydrogen barrier, e.g., silicon-rich oxide insulator (SILOX), are thereafter formed over the ferroelectric capacitors for protection thereof. The Udayakumar reference appears to describe fabrication of a control element, e.g., transistor, but does not utilize a silicon-rich oxide insulator in formation of the control element, e.g., transistor (see Figure 4A and related text).

In addition, Applicant has amended each of independent claims 1, 16, 26, 38, 47, and 55, to clarify the silicon-rich insulator limitation as being "configured to inject current into the tunnel junction when the memory cell is selected". The Udayakumar reference does not appear to describe, teach, or suggest this aspect of the claimed invention, and indeed cannot since the Udayakumar reference uses a silicon-rich

insulator in an entirely different application. From Applicant's review of the Miyasaka reference, the Miyasaka reference does not cure the deficiencies of the Udayakumar reference.

Furthermore, Applicant submits that the suggested motivation "to improve the characteristic's of the device" is merely conclusory and too general, since it may respectively be applied in an attempt to justify virtually any type of modification contemplated, and does not provide motivation for making the specific modification asserted. It is respectfully submitted that a *prima facie* case of obviousness has not been established, as no clear and particular evidence of motivation, or specific rational, to combine can be identified.

Applicant respectfully submits that one skilled in the art would not be motivated by the use of silicon-rich oxide insulator for protection of ferroelectric capacitors as taught in the Udayakumar reference, to fabricate a memory cell having a control element including a silicon-rich insulator configured to inject current into the tunnel junction when the memory cell is selected. Applicant respectfully submits that each and every element and limitation of independent claims 1, 16, 26, 38, 47, and 55, is not described taught, or suggested in the Miyasaka and Udayakumar references, either independently or in combination. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the 103 rejection of independent claims 1, 16, 26, 38, 47, and 55, as well as those claims that depend therefrom.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney Timothy F. Myers at (541) 715-4197.

At any time during the pendency of this application, please charge any additional fees or credit overpayment to the Deposit Account No. 08-2025.

CERTIFICATE UNDER 37 CFR §1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: **MS RCE** Commissioner for Patents, P.O. BOX 1450 Alexandria, VA 22313-1450, on this 14th day of September, 2007.

Alison L. Subendra
Name

Signature

Respectfully Submitted,
Peter J. Fricke, et al.

By Applicants' Representatives,
Brooks, Cameron & Huebsch, PLLC
1221 Nicollet Avenue, Suite 500
Minneapolis, MN 55403

By: _____
Edward J. Brooks III
Reg. No. 40,925

Date: 9/14/2007